Applicant:	Benedict G. Pace	Docket No:	NH-07a
Serial No.:	09/737,407	Group Art Unit:	2822
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Remarks

The specification has been amended on page 12, line 16 to better identify the copending application which has now issued as United States Patent 6,613,605.

Claims 16 and 19-22 were rejected as anticipated by Wood et al., U.S. 3,663,184. Wood et al. describe a barrier layers of titanium, titanium/nickel and nickel (col. 3, lines 64-70) to protect the semiconductor die from degradation by constituents of the solder bump. Wood et al. in col. 2, lines 10-15 specify that the bumps of their invention melt in the range of 361°**F** to 625°**F**, i.e., 182.8°**C** to 329.4°**C**. Applicant's claim 16 and dependent claims 17-24 teach the formation of solderable metal bumps by melting a metal having a melting point over 350°**C**, which applicant submits is not anticipated by Wood et al. Wood et al. is concerned with forming solder bumps on a semiconductor die, so the temperatures of bump formation must be carefully controlled to avoid damaging the die by excessive heat. Applicant's invention is concerned with a package for an electronic device, e.g. a semiconductor chip. The package is manufactured, and metal bumps are formed before the semiconductor device is mounted on the package, so the bumps may be formed of high melting metals that cannot be melted onto a semiconductor chip.

Wood et al., col. 3, lines 2-6, suggest gold-tin, lead-tin-gold and gold-indium solders could be employed using the same principles, i.e., melting in the range of 182.8° to 329.4°**C**. The eutectic alloy of gold-tin melts at 280°C. The melting point of lead is 327.5°C; tin melts at

232°C, and the lead-tin eutectic melts at 182.8°C. Only a slight amount of gold, ca. 2%, can be tolerated in lead-tin solder because the Au_3Sn_4 intermetallic makes lead-tin solders brittle and prone to fracture. The small gold content of useable lead-tin-gold alloys makes a negligible change in the melting point of the composition. The melting point of indium is 156°C, and gold melts at 1064°C. Gold-indium mixtures could melt anywhere between these two temperatures based on the varying percentage of gold and indium. There is no teaching in Wood et al. of utility of gold-indium solders having melting points over 329°C. Therefore applicant respectfully submits one skilled in the art following Wood et al., col. 2, lines 10-15; col. 2, lines 20-27, and col. 3 lines 5-10 would use the gold-tin eutectic solder, low melting tin-lead solders with less than 2% gold, or indium-gold mixtures melting under 329°C.

Applicant respectfully submits that Wood et al. show a lead-tin solder bump in Fig. 2d, not a gold bump, see col., lines 64-66. The gold layer merely serves as an etch resist and an adhesive layer for the solder bump, see col. 3, lines 34-40. The gold layer is thin, 1 micron thick (col. 3, line 45), and does not constitute a bump. Applicant respectfully submits that there is no disclosure by Wood et al. of copper bumps, rather, the only reference to copper, col. 3, line 68, implicitly acknowledges that copper is a common metal conductor on the support substrate to which the flip chip is bonded, see col. 1, lines 50-53. Based on the foregoing, applicant respectfully requests that the rejection of claims 16-24 under 35 USC § 102(b) be withdrawn.

Claims 17-18 were rejected over Wood et al. in view of Yamaji et al., U.S. 6,159,837.

Yamaji et al. screen-prints a eutectic solder (melting point 182°C) paste onto a semiconductor chip. Applicant submits that low temperature process of Yamaji et al. combined with Wood does not teach or suggest applicant's invention of depositing a powdered form of a metal having a melting point over 350°C, on metallic pads and melting the metal, forming bumps on the metallic pads. Wood et al., Yamaji et al. and Kondo et al. are all concerned with forming bumps on semiconductor dice. To prevent compromising the semiconductor dice they must use low temperature processes and low melting metals. Applicant teaches high temperature insulating materials (page, 8, line 20 of the specification), that may be used for an electronic package that will contain a semiconductor die (page 9, lines 17-18; Fig. 1 and page 12, lines 3-9 of the specification). Since the bumps are formed on the package before the die is inserted in the package, applicant has discovered he can use metals and alloys with high temperature melting points which provide reliable connections from the package to the next level interconnect. Applicant respectfully submits Woods et al., Yamaji et al. and Kondo et al. describe processes for forming bumped semiconductor die, which alone or in combination do not teach or suggest applicant's novel techniques for forming bumped substrates. Therefore applicant respectfully requests that the rejection of claims 17, 18, 23 and 24 under 35 USC §103 (a) be withdrawn.

The other prior art, which is of record but not relied on, has been reviewed. Applicant respectfully submits that these references do not teach or suggest the invention claimed by the

applicant.

New claims 25 to 38 have been added to more completely describe applicant's invention. New claims 25 and 28 find support in the specification on page 6, lines 15-19. New claims 26 and 31 are supported in the specification from page 14, line 22 to page 15, line 5. New claims 27 to 38 are supported by the Fig. 3 and its description in the specification from page 12, lines 18-23, and by original claims 16-24.

Applicant respectfully submits that claims 16-24 and new claims 25-38 describe novel methods of manufacturing electronic packages, and respectfully requests an early allowance.

Respectfully submitted

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